PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: GEOFFREY S. STRONGIN DALE E. GULICK	Conf. No. 6355 Examiner: A. Li
Serial No.: 09/853,225	Group Art Unit: 2183
Filed: May 11, 2001	Att'y Docket: 2000.038900
For: SECURE SYSTEM MODE DURATION MANAGEMENT	Customer No. 23720

APPEAL BRIEF

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final Office Action dated August 23, 2006. A Notice of Appeal was filed on November 9, 2006 and so this Appeal Brief is timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500) from **Williams, Morgan & Amerson's P.C. Deposit Account 50-0786/2000.038900.**

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc. The assignment of the present application to Advanced Micro Devices, Inc., is recorded at Reel 011816, Frame 0527.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-3, 5-14, and 16-33 are pending in the present application. Claims 1-2, 5-13, and 16-33 stand rejected under 35 U.S.C. § 102(b) as allegedly being obvious over Walker, et al (U.S. Patent No. 5,771,390) in view of Angelo, et al (U.S. Patent No. 6,581,162). Claims 3 and 14 stand rejected under 35 U.S.C. § 102(b) as allegedly being obvious over Walker in view of Angelo and admitted prior art.

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1 and 12 set forth an indicator configured to indicate when the computer system is in a secure operating mode, a first timer configured to indicate a duration in which the indicator is active, and control logic coupled to receive the duration from the first

timer. The control logic is configured to provide a control signal upon the duration reaching a predetermined value. For example, in on embodiment, control logic 420 is coupled to control operation of an SMM timing controller 401A, an SMM access controller 402A, and an SMM initiator 425A. Input and output (I/O) to security hardware 370A pass through the SMM access filters 410 and are routed through the control logic 420A. The SMM timing controller 401A includes a kick-out timer 407A that counts down from a predetermined value while the computer system 100 is in SMM. The control logic 420A is configured to assert a control signal (EXIT SMM 404) for the processor to exit SMM, such as in response to the expiration of the kick-out timer 407A. The restart timer 408, included in the SMM timing controller 401A, starts counting down from a predetermined value after the kick-out timer 407A reaches zero. The SMM indicator 405, also included in the SMM timing controller 401A, is operable to monitor the status of one or more signals in the computer system, such as the SMI# (System Management Interrupt) signal and/or the SMIACT# (SMI ACTive) signal to determine if the computer system is in SMM. See Patent Application, page 19, ll. 6-21 and Figure 5A.

Independent claims 25, 28, and 31 set forth determining if the computer system is in a secure operating mode, initiating a first timer if the computer system is in the secure operating mode, and determining if the first timer has reached a predetermined value. Independent claims 25, 28, and 31 also set forth asserting a control signal if the first timer has reached the predetermined value. For example, one embodiment of a method described in the specification includes checking if the computer system is in SMM in decision block 905. If the computer system is in SMM in decision block 905, then the method initiates a kick-out timer 407 in block 910. The method next checks to determine if the kick-out timer 407 has expired in decision block 915. If the kick-out timer 407 has expired in decision block 915, then the method

transmits a request to the processor to exit SMM without completing the SMI request that invoked SMM, in block 920. See Patent Application, page 37, line 23 – page 38, line 4 and Figure 10A.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully requests that the Board review and overturn the two rejections present in this case. The following issues are presented on appeal in this case:

(A) Whether claims 1-2, 5-13, and 16-33 are obvious over Walker in view of Angelo; and

(B) Whether claims 3 and 14 are obvious over Walker in view of Angelo and admitted prior art.

VII. ARGUMENT

A. Legal Standards

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573

(Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id*. at 1434-35. Moreover, it is the claimed invention, as a whole, that must be considered for purposes of determining obviousness. A mere selection of various bits and pieces of the claimed invention from various sources of prior art does not render a claimed invention obvious, unless there is a suggestion or motivation in the prior art for the claimed invention, when considered as a whole.

B. Claims 1-2, 5-13, and 16-33 are not obvious over Walker in view of Angelo.

Walker describes techniques for triggering the transition of a computer from a suspend state to a suspend-to-disk state. The suspend state and the suspend-to-disk state are states used in power management that consume varying amounts of power. For example, the suspend state results in a large number of components and peripherals receiving reduced or no power. The suspend-to-disk state causes power to the computer system to be completely removed. Timers or

clocks are typically disabled in the suspend state, which may make it difficult to implement this state in a manner that permits later transition to the suspend-to-disk state. See Walker, col. 1, line 38-col. 2, line 16. Accordingly, Walker describes setting a real-time clock alarm prior to placing the computer in the suspend state. When the real-time clock alarm expires, the computer system may transition from the suspend state to the suspend-to-disk state. See Walker, col. 5, line 59-col. 6, line 57 and Figure 3. However, as admitted by the Examiner at paragraph 13 on page 8 of the Office Action, Walker does not teach or suggest any operating modes of the computer that include secure operating modes. Accordingly, Walker does not teach or suggest using the real-time clock alarm to determine a duration of a secure operating mode.

The Examiner relies upon Angelo to describe a system management mode that may be used to implement a secure operating mode. Angelo describes techniques for creating, storing, and using encryption keys in a distributed computing environment. In particular, Angelo describes system management interrupts that may be asserted by a system management interrupt timer, by a system requests, or by other means. A system management interrupt active signal may be provided by a processor to indicate operation in a system management mode. See Angelo, col. 7, line 55 – col. 8, line 11. However, Angelo does not (explicitly or inherently) describe or suggest a timer configured to indicate a duration of a secure operating mode.

Thus, Applicants respectfully submit that neither Walker nor Angelo teaches or suggests a timer configured to indicate a duration of a secure operating mode. Accordingly, Applicants respectfully submit that the prior art of record fails to teach or suggest all the limitations set forth in independent claims 1, 12, 25, 28, and 31.

Applicants further submit that neither Walker nor Angelo provide any suggestion or motivation to modify the prior art of record to arrive at the claimed invention. In the Final

Office Action, the Examiner alleges that Walker describes using timers to determine when to enter and/or exit certain power management modes, such as the system management mode. The Examiner also alleges that Angelo describes the use of the system management mode to provide computer security and alleges that this corresponds to operating the system in a secure mode. The Examiner then alleges that the combination of Walker and Angelo suggests the use of timers configured to indicate durations of secure operating modes. Applicants respectfully disagree. As discussed above, the timers described by Walker are used to determine when to transition between power management modes because pre-existing timers may be disabled in certain power management modes. However, the prior art does not teach or suggest that the pre-existing timers are disabled in different secure modes and, in particular, neither Walker nor Angelo teaches that the techniques described in Angelo affect power consumption in any way. Thus, neither Walker nor Angelo describe or suggest any need for implementing additional timers to indicate how long a system is in a secure mode. Applicants therefore submit that the prior art of record fails to provide any suggestion or motivation for a timer configured to indicate a duration of a secure operating mode, as set forth in independent claims 1, 12, 25, 28, and 31.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over the prior art of record and request that the Examiner's rejections of claims 1-2, 5-13, and 16-33 under 35 U.S.C. 103(a) be withdrawn.

C. Claims 3 and 14 are not obvious over Walker in view of Angelo and admitted prior art.

Claims 3 and 14 depend from independent claims 1 and 12, respectively. As discussed above, neither Walker nor Angelo teaches or suggests a timer configured to indicate a duration of a secure operating mode, as set forth in independent claims 1 and 12. The Examiner notes that the admitted prior art describes a south bridge. However, the admitted prior art fails to remedy the aforementioned fundamental deficiencies of Walker and Angelo. Thus, for at least the reasons discussed above with respect to independent claims 1 and 13, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over the prior art of record and request that the Examiner's rejections of claims 3 and 14 under 35 U.S.C. 103(a) be withdrawn.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-3, 5-14, and 16-33 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix for this appeal.

XI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-3, 5-14, and 16-33, over the prior

art of record. The undersigned may be contacted at (713) 934-4052 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

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AGENT FOR APPLICANTS

CLAIMS APPENDIX

1. (Previously Presented) A device configured for use in a computer system, comprising:

an indicator configured to indicate when the computer system is in a secure operating mode;

a first timer configured to indicate a duration in which the indicator is active; and

control logic coupled to receive the duration from the first timer, wherein the control logic is configured to provide a control signal upon the duration reaching a predetermined value.

2. (Original) The device of claim 1, wherein the device includes a bridge.

3. (Original) The device of claim 2, wherein the bridge includes a south bridge.

4. (Canceled)

5. (Previously Presented) The device of claim 1, wherein the secure operating mode includes system management mode (SMM).

6. (Previously Presented) The device of claim 1, wherein the control signal is configured to indicate that the computer system should exit the secure operating mode.

7. (Original) The device of claim 1, wherein the predetermined value less than about 2 seconds.

8. (Original) The device of claim 7, wherein the predetermined value is not substantially less than 200 milliseconds.

9. (Original) The device of claim 1, wherein the predetermined value is set by software or firmware executing in the device.

10. (Original) The device of claim 1, further comprising:

a second timer configured to indicate a duration since the control signal has been provided;

wherein the control logic is further coupled to receive an indication from the second timer of the duration, wherein the control logic is further configured to provide a second control signal upon the duration since the control signal has been provided reaching a second predetermined value.

11. (Original) The device of claim 10, wherein the second control signal is configured to indicate that the computer system should enter the secure operating mode.

12. (Previously Presented) A computer system, comprising:

a processor; and

a device coupled to the processor, wherein the device includes:

an indicator configured to indicate when the processor is in a secure operating mode;

a first timer configured to indicate a duration in which the indicator is active; and

control logic coupled to receive the duration from the first timer, wherein the control logic is configured to provide a control signal to the processor upon the duration reaching a predetermined value.

13. (Original) The computer system of claim 12, wherein the device comprises a bridge.

14. (Original) The computer system of claim 13, wherein the bridge comprises a south bridge.

15. (Canceled)

16. (Previously Presented) The computer system of claim 12, wherein the secure operating mode includes SMM.

17. (Previously Presented) The computer system of claim 12, wherein the control signal is configured to indicate that the processor should exit the secure operating mode.

18. (Original) The computer system of claim 12, wherein the predetermined value less than about 2 seconds.

19. (Original) The computer system of claim 18, wherein the predetermined value is not substantially less than 200 milliseconds.

20. (Original) The computer system of claim 12, wherein the predetermined value is set by software or firmware executing in the device.

21. (Original) The computer system of claim 12, wherein the device further comprises:

a second timer configured to indicate a duration since the control signal has been provided;

wherein the control logic is further coupled to receive an indication from the second timer of the duration, wherein the control logic is further configured to provide a second control signal upon the duration since the control signal has been provided reaching a second predetermined value.

22. (Original) The computer system of claim 21, wherein the second control signal is configured to indicate that the processor should enter the secure operating mode.

23. (Original) The computer system of claim 22, wherein the device further comprises:

a register coupled to receive a jump address for an interrupt, wherein the jump address corresponds to the processor entering the secure operating mode.

24. (Original) The computer system of claim 23, wherein the interrupt comprises an SMI, wherein the secure operating mode comprises SMM.

25. (Previously Presented) A method for operating a computer system, the method comprising:

determining if the computer system is in a secure operating mode;

initiating a first timer if the computer system is in the first operating mode;

determining if the first timer has reached a predetermined value; and

asserting a control signal if the first timer has reached the predetermined value.

26. (Previously Presented) The method of claim 25, wherein determining if the computer system is in a secure operating mode includes determining if the computer system is in system management mode, and wherein asserting a control signal if the first timer has reached the predetermined value includes executing an RSM instruction before an SMI handler exits the system management mode.

27. (Original) The method of claim 26, further comprising:

issuing an SMI request;

the computer system entering system management mode; and

the SMI handler servicing the SMI request;

wherein executing an RSM instruction before an SMI handler exits the system management mode occurs while the SMI handler is servicing the SMI request.

28. (Previously Presented) A method for operating a computer system, the method comprising:

step for determining if the computer system is in a secure operating mode;

step for initiating a first timer if the computer system is in the secure operating mode;

step for determining if the first timer has reached a predetermined value; and

step for asserting a control signal if the first timer has reached the predetermined value.

29. (Previously Presented) The method of claim 28, wherein the step for determining if the computer system is in a secure operating mode includes step for determining if the computer system is in system management mode, and wherein the step for asserting the control signal if the first timer has reached the predetermined value includes step for executing an RSM instruction before an SMI handler exits the system management mode.

30. (Original) The method of claim 29, further comprising:

step for issuing an SMI request;

step for the computer system entering system management mode; and

step for the SMI handler servicing the SMI request;

wherein the step for executing an RSM instruction before an SMI handler exits the system management mode occurs while the SMI handler is servicing the SMI request.

31. (Previously Presented) A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of operating the computer system, the method comprising:

determining if the computer system is in a secure operating mode;

initiating a first timer if the computer system is in the secure operating mode;

determining if the first timer has reached a predetermined value; and

asserting a control signal if the first timer has reached the predetermined value.

32. (Previously Presented) The computer readable program storage device of claim 31, wherein determining if the computer system is in a secure operating mode includes determining if the computer system is in system management mode, and wherein asserting a control signal if the first timer has reached the predetermined value includes executing an RSM instruction before an SMI handler exits the system management mode.

33. (Original) The computer readable program storage device of claim 32, the method further comprising:

causing an SMI request to be issued;

wherein executing an RSM instruction before an SMI handler exits the system management mode occurs while the SMI handler is servicing the SMI request.